Single-ended Differential Amplifier and Mixer Circuits Utilizing Complementary RF Characteristics of both NMOS and PMOS

Ilku Nam, Bonkee Kim, and Kwyro Lee

Dept. of EECS, Korea Advanced Institute of Science and Technology, Also with MICROS Research Center, 373-1 Guseong-dong, Yuseong-gu, Daejeon, 305-701, Korea

Abstract — **Design and fabrication results for single-ended differential circuit topologies that utilize the complementary RF characteristic of both NMOS and PMOS are reported. The complementary CMOS parallel push-pull amplifier gives an order of magnitude improvement in IP_2 at similar power consumption, and single-balanced complementary resistive mixer that functions effectively as double-balanced one, improves similar order of magnitude better in IP_2, LO-to-IF and LO-to-RF isolations than NMOS counterparts.**

I. INTRODUCTION

CMOS circuit composed of NMOS and PMOS devices is perhaps considered as the most ingenious circuit topologies ever invented, providing the best speed per power performance. There are two famous CMOS circuits, that is, the static CMOS circuit and the class B push pull amplifier. Though CMOS has the best symmetrical characteristics among complementary device families, its asymmetry is appreciable. In digital CMOS, for example, the size of PMOS is chosen to be about 2.5 times as large as that of NMOS. This causes the increase of total effective parasitic capacitance, so the speed of CMOS digital circuit is inferior to that of digital circuit consisting mostly of NMOS. Nevertheless, the static CMOS is the most popularly used digital circuit.

RF core circuits have hardly adopted PMOS because of its poor RF performance. Although it is true that PMOS has much lower current driving capability than NMOS, however, we found that its small signal RF performance is good enough to be used in RF circuits [1]. So, the complementary characteristics of NMOS and PMOS can indeed be fully utilized in RF core circuits without significant RF performance degradation. Actually, there have been several efforts to use PMOS in RF core circuit element and analog circuits, such as PMOS cross-coupled pair [2] and NMOS cross-coupled pair stacked with PMOS cross-coupled pair [3] to generate negative resistance for VCO, an active load to replace large size inductor load [4], and analog operational amplifier [5], etc. However, these are limited only to either oscillator or low frequency circuits. To the author's knowledge, there has been no report on CMOS amplifier and mixer utilizing RF performance of both NMOS and PMOS device in a truly complementary fashion.

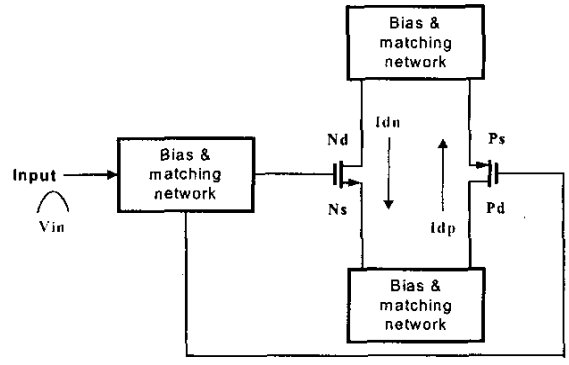

Fig. 1. Schematic of the generic single-ended differential RF circuits using complementary devices

Recently, the direct conversion receiver and low-IF receiver have drawn attention as a possible solution to implement a single-chip receiver with integrated digital modem blocks [6][7]. In these receivers, IP_2 as well as IP_3 is an important parameter indicating immunity to various interferences. Thus, these receivers prefer to use differential circuit topology. However, one of the obstacles for differential scheme is that baluns are required to convert single-ended signal to differential signals and vice versa. There are two types of balun, i.e., active and passive type. Though active balun is good for integration, it does not provide the accuracy. So, passive balun is practically used. For the frequency range of few GHz, however, passive balun is too large to be integrated on a chip. Moreover, it is difficult to have wideband balun. Therefore it is important to have differential circuits without balun.

In this paper, we propose the amplifier and mixer circuits for wireless RF application that fully utilize both NMOS and PMOS devices. These circuits provide the single-ended differential signal processing and alleviate the use of the baluns.

0-7803-7694-3/03/$17.00 © 2003 IEEE

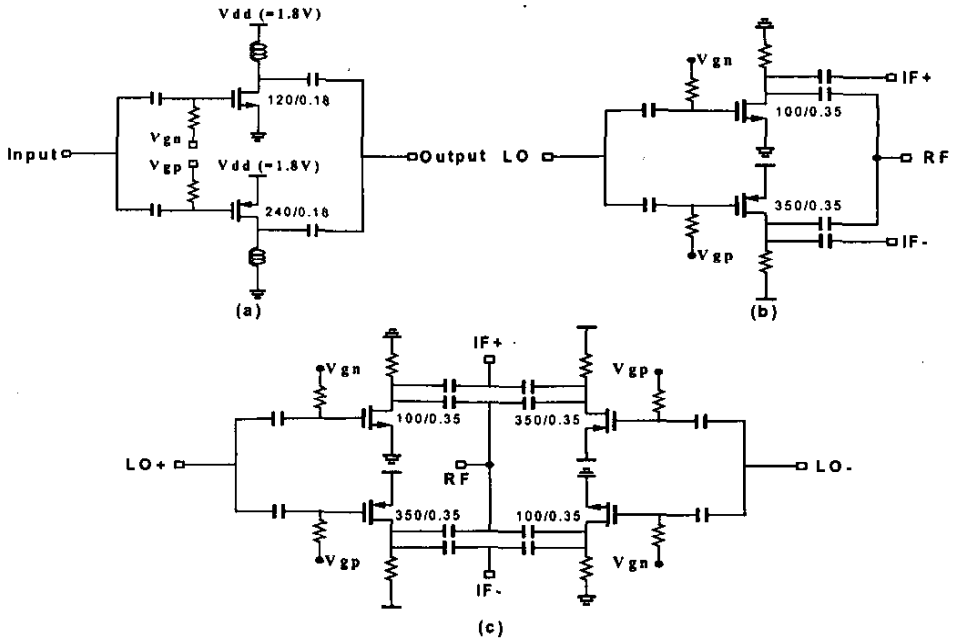

Fig. 2. (a) Schematic of CCPP (Complementary CMOS Parallel Push-pull) amplifier, (b) Schematic of UCR (Unbalanced Complementary Resistive) mixer, (c) Schematic of SCR (Single-ended Complementary Resistive) mixer

II. Single-Ended Differential RF Signal Processing Methods Using Complementary Devices

Fig. 1 shows the generic schematic of single-ended *differential circuit topology using complementary devices* [1][8]. In this figure, though the input signal is tied together at the gates of NMOS and PMOS, the core is operating as the differential mode because of the complementary action of NMOS and PMOS. When the outputs at drain nodes of NMOS and PMOS are tied together, we can obtain the single-ended output, because they have the same phase. The situation is the same when both the source nodes are used as the output ports. In these cases, the input is single-ended, the core operates as differential, and the output is single-ended again. However, it is interesting to note that the differential (out-of-phase) outputs can also be obtained by selecting Nd and Ps, and vice versa. In summary, by selecting the in-phase nodes as the outputs, it is possible to implement the single-ended differential amplifier, which eliminates even order distortion without input and output baluns. On the other hand, by selecting out-of-phase outputs, it is possible to implement the mixer, which has the single-ended input and differential output. Consequently, the single-ended differential signal processing is possible. It ameliorates IP_2 and the isolation characteristic without the use of the balun. Especially, this is important in the wideband RF system and for monolithic integration.

III. High IP_2 Amplifier and Differential Mixer Circuits Using Complementary Characteristic of CMOs

Fig. 2(a) shows the schematic of CCPP (Complementary CMOS parallel push-pull) amplifier invented on the basis of the concept in section II. Note that both NMOS and PMOS circuits are combined in parallel between ground and power supply lines, which is in contrast with CMOS static digital and push pull amplifier circuit combined in series. Therefore CCPP amplifier is suitable for low voltage. In CCPP, we can make the transconductance nonlinearity of NMOS, i.e., gm′ of NMOS to be cancelled by that of PMOS using proper gate bias and transistor size, which can suppress 2nd order nonlinearity and improve IP_2 drastically [1]. Though CCPP cannot improve IP_3 in principle, we found IP_3 improves several dB due to other 3rd order cancellation effect.

Fig. 2(b) and (c) show the unbalanced complementary resistive (UCR) mixer and the single-balanced

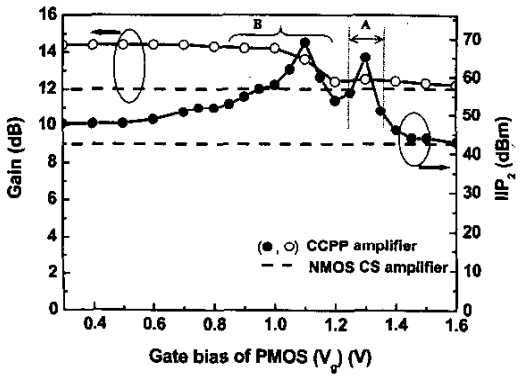

Fig. 3. Measured gain and IIP_2 of CCPP amplifier and NMOS common source (CS) amplifier (Solid and dashed lines are for CCPP and NMOS CS amplifier, respectively. Power supply voltage is 1.8V.)

Table 1. Measured performance summaries of NMOS CS and CCPP amplifier

	NMOS CS amplifier	CCPP amplifier
Gain	12dB	12.4dB
NF	1.9dB	2.0dB
IIP_2	43dBm	56dBm
IIP_3	7.5dBm	8.1dBm
Power consumption	14.04mW @1.8V	14.91mW @1.8V
F.O.M. (Linearity) $(=10(\log\frac{OIP_2(mW)}{P_{DC}(mW)}+\log\frac{OIP_3(mW)}{P_{DC}(mW)}))$	51.6dB	65.4dB

complementary resistive (SCR) mixer using our concept. The UCR mixer functions effectively as single balanced mixer. Thus, compared with conventional unbalanced NMOS resistive (UNR) mixer, the UCR mixer does not use differential LO signals, has smaller LO leakage at IF outputs, larger IP_2 and conversion gain. However, large common mode LO signal still exists. This can greatly be alleviated by using the SCR mixer, which functions effectively as double balanced mixer. There is neither LO leakage at IF port nor at RF port. This improves both LO-IF and LO-RF isolation. The SCR mixer circuit is very plausible for single chip integration because it requires neither RF nor LO balun since well-balanced LO signals are usually available from VCO easily.

IV. Experimental Results

The measured gain and IIP_2 of CCPP amplifier and NMOS common source (CS) amplifier are shown in Fig. 3. Measurement is done at RF frequency of 2.1GHz and 2.11GHz for NMOS V_{gs} of 0.7V and V_{dd} of 1.8V, changing the gate bias of PMOS from 0.3V to 1.6V. In Fig. 3, IP_2 values increase significantly as large as 26dB and showing two peaks, one is in the sub-threshold region (indicated as A) and another in strong inversion region (indicated as B). In A, PMOS is operating in the subthreshold regime. Thus it neither increases the gain, nor the power consumption. In B, however, it is operating in strong inversion regime, leading to about 3dB gain increase with additional power consumption. Fig. 3 shows the IP2 of CCPP amplifier improve at least 10dB over a wide bias window for both regions enough to cover the process variation. On the other hand, it is possible to increase IP_3 by adding MGTR (Multiple Gated Transistors) to CCPP, if necessary [9]. Table 1 shows that the CCPP amplifier has better figure of merit for linearity than NMOS counterpart. Noise figure of CCPP amplifier degrades slightly by 0.1dB from 1.9dB of NMOS CS amplifier.

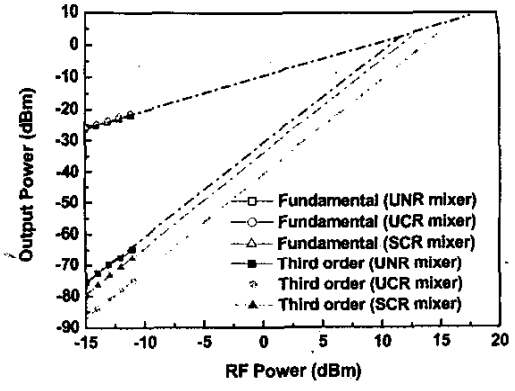

Fig. 4. IP_3 measurement plot for resistive mixers

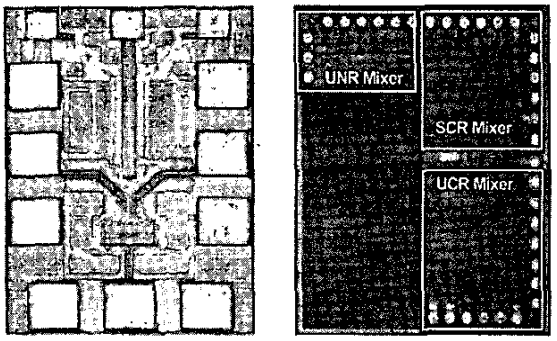

Fig. 5. Chip photographs of (a) CCPP amplifier and (b) complementary resistive mixers

Fig. 4 shows the IP_3 measurement plot of resistive mixers when two tones at 2.1GHz and 2.101GHz are mixed with the LO frequency of 2.097GHz at the LO power of 4dBm. Table 2 shows that the UCR mixer has about 5dB better IIP_2, 4dB better IIP_3 and 15dB better LO-IF isolation than NMOS counterpart. Moreover, the SCR mixer provides 10dB better IIP_2, 1.5dB better IIP_3, 20dB better LO-IF isolation, and 18dB better LO-RF isolation. As shown in Table 2, the proposed complementary resistive mixers have relatively better performance than other NMOS resistive mixers published.

The CCPP amplifier shown in Fig. 5(a) has been fabricated in TSMC 0.18μm CMOS process and the resistive mixers shown in Fig. 5(b) have been fabricated in 3-metal layer 0.35μm CMOS process.

V. Conclusion

In this paper, the RF circuits that fully utilize the advantages of complementary devices are proposed. The complementary nature of these circuits inherently provides single-ended differential signal processing capability, alleviates the use of balun or differential signal generating circuits. In addition, these have good RF performance, that is, CCPP amplifier has more than 10dB IP_2 improvement than NMOS CS amplifier with little additional power consumption and the complementary resistive mixers have better linearity and port isolation characteristics than NMOS counterparts. These proposed circuit topologies are expected to be a viable choice for integration of RF circuits in a single chip.

Acknowledgement

This research is supported by the MICROS (Micro Information and Communication Remote Object-Oriented Systems) Research Center.

References

[1] B. Kim, I. Nam, and K. Lee, "Single-ended Differential RF Circuit Topologies Utilizing Complementary MOS Devices", *Journal of Semiconductor Technology and Science,* vol. 2, no. 1, pp. 7-18, Mar. 2002.

[2] J. J. Kucera, "Wideband BiCMOS VCO for GSM/UMTS direct conversion receivers", *ISSCC Digest of Technical Papers*, pp. 374-375, Feb. 2001.

[3] D. Ham and A. Hajimiri, "Concept and methods in optimization of integrated LC VCOs", *IEEE Journal of Solid-State Circuits,* vol. 36, no. 6, pp.896-909, 2001

[4] R. Gupta, B. M. Ballweber, and D. J. Allstot, "Design and optimization of CMOS RF power amplifiers", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 2, pp. 166-175, 2001

[5] K. D. Langen and J. H. Huijsing, COMPACT LOW-VOLTAGE AND HIGH-SPEED CMOS, BiCMOS AND BIPLOAR OPERATIONAL AMPLIFIERS, Kluwer Academic Publishers, 1999

[6] D. Manstretta, R. Castello, F. Gatta, P. Rossi, and F. Svelto, "A 0.18μm CMOS Direct-Conversion Receiver Front-End for UMTS," *ISSCC Digest of Technical Papers,* pp. 234-235, Feb. 2002.

[7] Y. J. Kim, H. Park, I. Nam, and K. Lee, "Architecture and algorithm for ultra-high precision image rejection mixer using digital compensation," *IEE Electronics Letters,* vol. 36, no. 19, pp. 1064-1066, Sept. 2000.

[8] K. Lee, and B. Kim, "Parallel Push-Pull Amplifier Using Complementary Device", US Patent 6087900, 2000

[9] B. Kim, J. Ko, and K. Lee, "A New Linearization Technique for MOSFET RF Amplifier Using Multiple Gated Transistors", *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 9, pp. 371-374, 2000

Table 2. Measured performance summaries and comparison of resistive mixers

	A. Shahani, 1997	K. Schmidt, 1998 (simulation)	P. Gould, 2000	UNR mixer	UCR mixer	SCR mixer
Operating frequency	1.4GHz	2.3GHz	1.8GHz	2.1GHz	2.1GHz	2.1GHz
LO power	0dBm	5dBm	4dBm	4dBm	4dBm	4dBm
Conversion gain (power gain)	- 3.6dB (voltage gain)	- 9dB	-6.9dB	-8.5dB	-7.9dB	-8dB
NF	-	-	-	8.9dB	8.4dB	8.4dB
IIP_2	-	-	-	42dBm	47dBm	53dBm
IIP_3	10dBm	14dBm	11.1dBm	11.5dBm	16dBm	13dBm
LO-to-IF isolation	-	-	43dB	25dB	40dB	46dB
LO-to-RF isolation	-	-	-	21dB	17dB	39dB
Technology	0.35μm CMOS	0.5μm CMOS	0.25μm CMOS	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS